ABSTRACT

0030 A method for forming a dual damascene structure in a semiconductor device manufacturing process including providing a process wafer including a via opening extending through at least one dielectric insulating layer; blanket depositing a negative photoresist layer to include filling the via opening; blanket depositing a positive photoresist layer over and contacting the negative photoresist layer; photolithographically patterning the positive photoresist layer to form a trench opening etching pattern overlying and encompassing the via opening; etching back the negative photoresist layer to form a via plug having a predetermined thickness; and, etching a trench opening according to the trench opening etching pattern.